# *EE/CprE/SE 492 BIWEEKLY REPORT 5*

***Date:*** ***October 26th, 2023 – November 8th, 2023***

***Group number:*** ***sddec23-08***

***Project title:*** ***ReRAM Compute ASIC Fabrication***

***Client &/Advisor:*** ***Henry Duwe & Cheng Wang***

***Team Members/Role:***

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

## Biweekly Summary

Over this past week, we have made more progress on the completion of our senior design project. After some talking and reflection, we have made a few last key changes to our circuit schematic. We changed some of the logic to the input of our “bitline” so that it could properly accommodate the voltages that are needed there. We also made some changes to the output of the “sourceline” so that we could ensure we were outputting the correct voltages to the harness. We walked through our circuit schematic, wrote out all the operations that would be done on the crossbar, and ensured that everything checked out.

With these updates, we also made more progress on the top-level simulation of our design. We are still essentially black-boxing the ReRAM as we can not simulate it, but we are using regular resistors to model the expected conductance of it. We have not gotten concrete results yet, but we are hoping to have core simulations as well as corner testing done by the middle of next week.

Along with simulations, we have gotten a jump start on creating the layouts for our overall design. We have successfully created an 8x8 crossbar of the ReRAM that passed both DRC and LVS checks. We have also created a layout for a 2x2 crossbar with larger transistor sizes for characterization. Layouts have also been created for the 8-line inputs for the worldline, bitline, and sourceline. All of these have passed DRC and LVS checks.

This week, we also tried to run a test case of pushing a 1T1R cell through the precheck. As was suspected, it failed precheck. After some troubleshooting, we figured out that this was not our fault and is the fault of the ReRAM symbol model that is currently a part of the Open PDKS, which is what Efabless provides to us. We have submitted a bug report on this issue and are waiting to get it fixed before the end of the semester, hopefully. We also created a model of the quantization of our design. We have found that a threshold of 1 is what is best for our design so as to get the best results we can from our design.

## Past Weeks Accomplishments

- Joshua Thater
    - Created layout of 8x8 crossbar
    - Created layout of “large” 2x2 crossbar
    - Created layout of 8 line bit line, word line, and source line inputs.
    - Updated schematic once more
    - Walked through operations on schematic to make sure that everything is able to be completed
- Aiden Petersen
    - Updated drivers to match new crossbar design
    - Modeled output in software
    - Simulated accuracy of quantization on convolutional neural network
    - Ran (and failed) pre-check on reram.
    - Documented pre-check
- Matt Ottersen
    - Created schematic and testbench for Control circuit for a 1T1R cell
    - Started working on simulation plan
    - Started simulations on testbench
- Regassa Dukele
    - Completed the layout for a 3-bit ADC
    - Start working on the integration and post-layout simulation

## Pending Issues

- Finish figuring out simulations on our design
- How we are going to fully hook everything up

## Individual Contributions

| Team Member | Individual Contributions | BIweekly Hours | Total Hours |
|---|---|---|---|
| Joshua Thater | Created layouts of crossbar, and 8 line inputs. Also, updated schematic and operations on it. | 21 | 160 |
| Aiden Petersen | Driver and design “finalization”, design simulations to test accuracy, pre-check stuff. | 15 | 110 |
| Matt Ottersen | Created Testbench for analog control and started running simulations | 14 | 110 |
| Regassa Dukele | Completed the layout for a 3-bit ADC and worked on post-layout simulation | 13 | 113 |

## Plans for the Upcoming Weeks

- Joshua Thater
    - Create layout for 8 Line source output
    - Hook up entire design in Caravan Harness and pass LVS and DRC checks
    - Work on documentation and bring up plan
    - Help with simulations if needed
- Aiden Petersen
    - Document everything I’ve done
    - Organize work into repositories
- Matt Ottersen
    - Finish simulations for the 1T1R cell
    - Scale design and run simulations for an 8x8 Testbench
- Regassa Dukele
    - Finish integration and post-layout simulation for 3-bit ADC
    - Work on simulation components with the team